120V N-Ch Power MOSFET

V_{DS}	120	V
$R_{DS(on),typ}$	1.8	m
$I_{D\ (Sillicon\ Limited)}$	341	A

			Value	Unit
	I_D		341	A
		T_C=100℃	241	
Drain to Source Voltage		-	120	V
Gate to Source Voltage	V_{GS}			
Pulsed Drain Current	I_{DM}			
Avalanche Energy, Single Pulse	E_{AS}			
Power Dissipation	P_D			
Operating and Storage Temperature	T_J, T_{stg}		-55 to175	℃

Absolute Maximum Ratings

	Symbol
Thermal Resistance Junction-Case	

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	120	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	2.0	2.9	4.0	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=120V, T_j=25℃	-	-	10	A
		V_{GS}=0V, V_{DS}=120V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	1.8	2.2	m
Transconductance				90	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz			-	

Dynamic Characteristics

Input Capacitance			-	10810	-	
Output Capacitance	C_{oss}		-		-	pF
Reverse Transfer Capacitance			-	20	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=60V, I_D=20A, V_{GS}				
Reverse Recovery Time	t_{rr}	V_R=60V, I_F=20A, dI_F/dt=100A/ s		95	-	ns
Reverse Recovery Charge	Q_{rr}		-	209	-	nC

Fig 1. Typical Output Characteristics

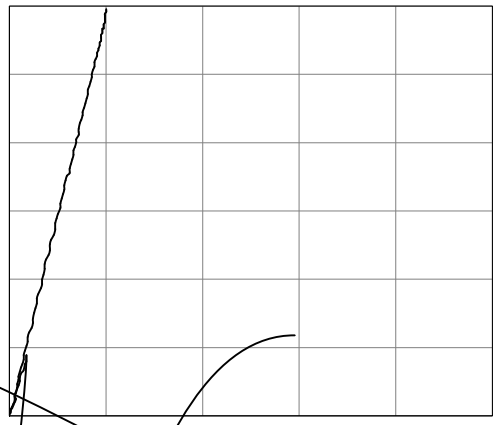


Figure 2. On-Resistance vs. Gate-Source Voltage

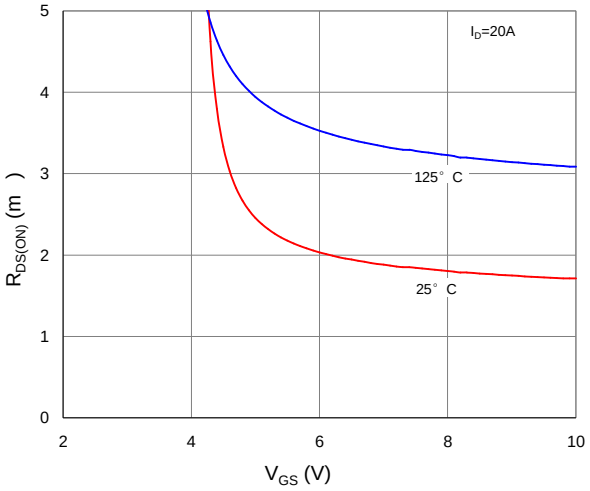


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

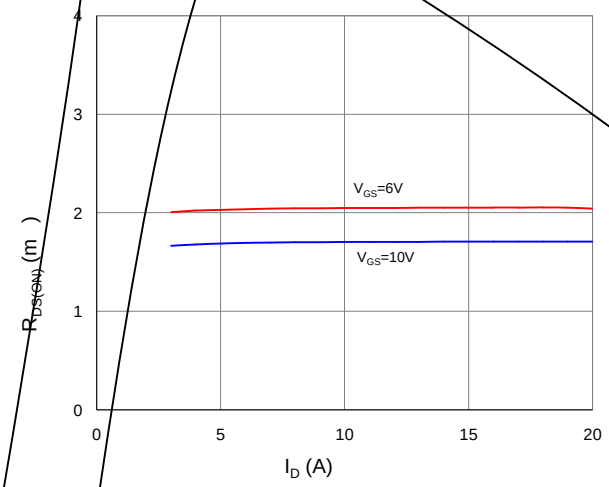


Figure 4. Normalized On-Resistance vs. Junction Temperature

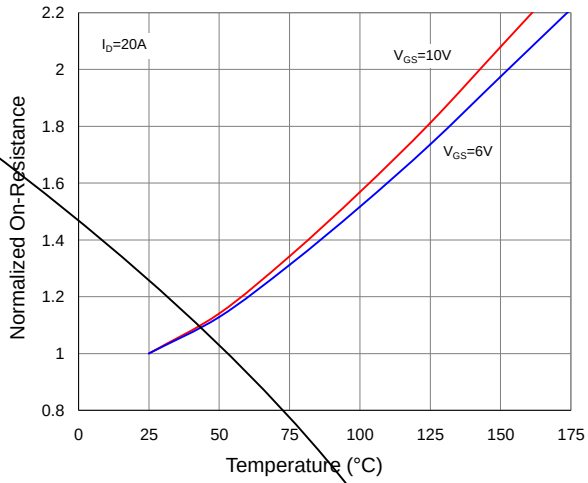


Figure 5. Typical Transfer Characteristics

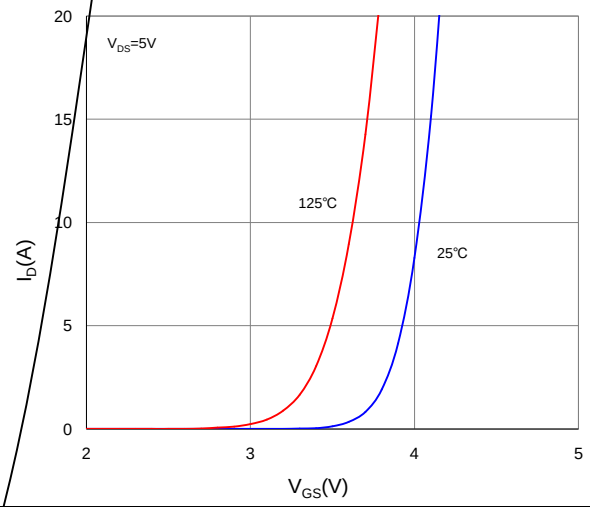


Figure 6. Typical Source-Drain Diode Forward Voltage

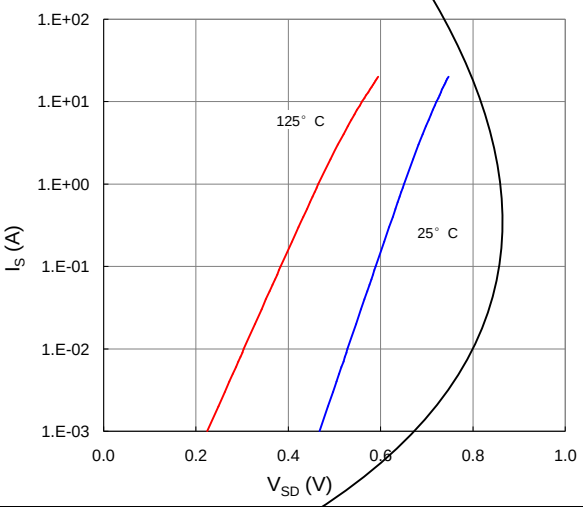


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

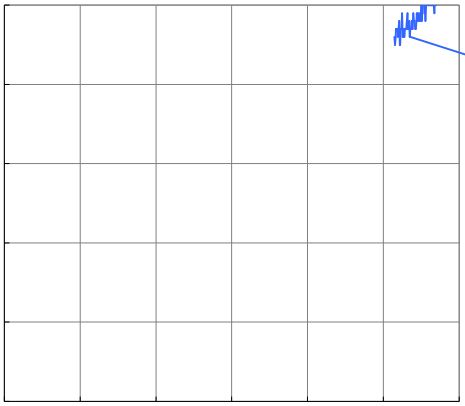
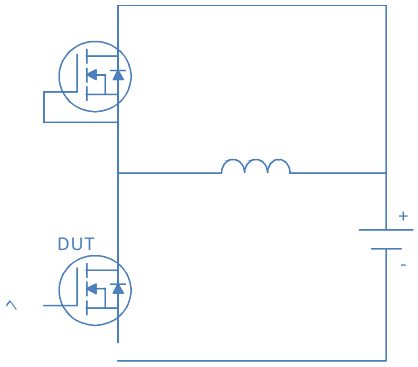
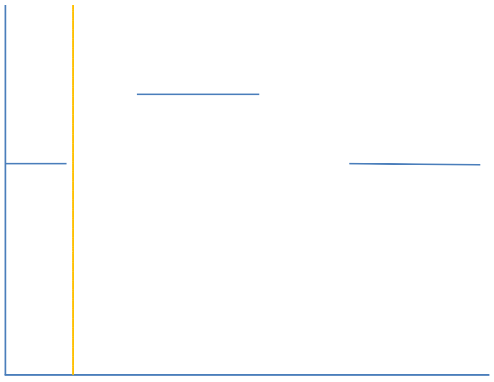


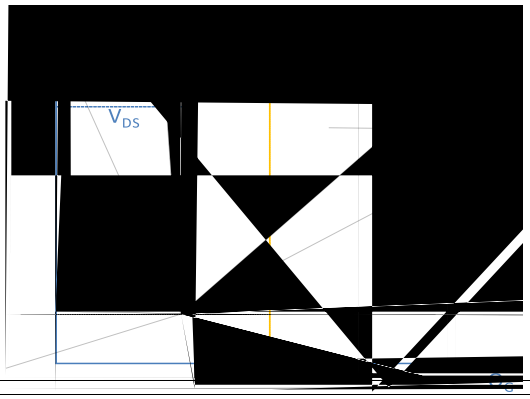
Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

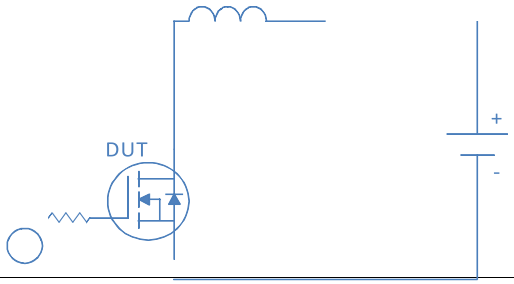
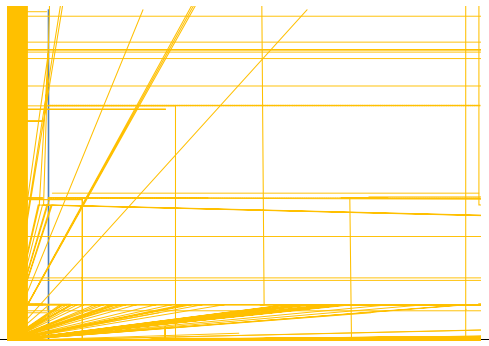
Figure 9. Maximum Safe Operating Area

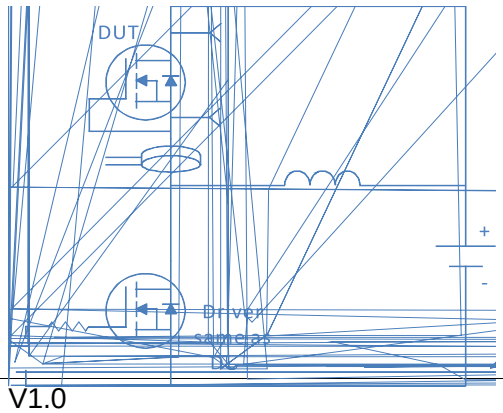
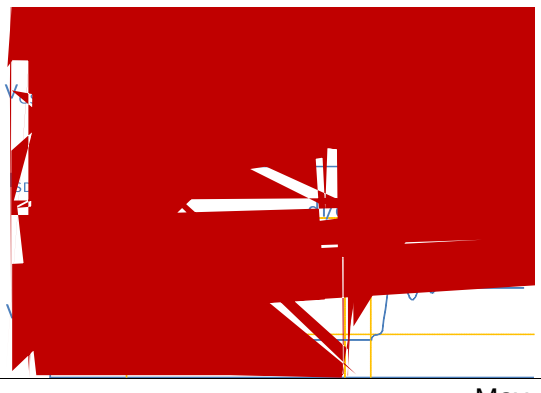
Figure 10. Maximun Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test	
	

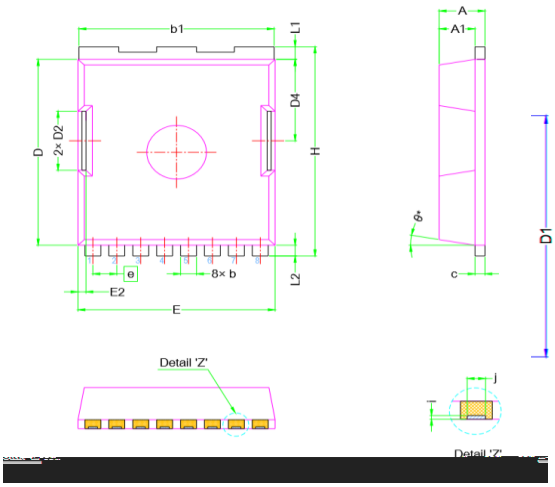
Gate Charge Test	
	

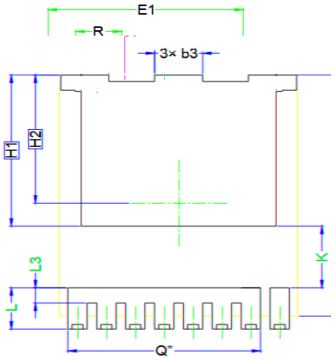
Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	
	

Package Outline

TOLL, 8 leads





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.90	2.00	2.10
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
E2	0.30	0.40	0.50
e	1.20 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
H2	5.89 BSC		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.60	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.60	0.70	0.80
N	8		
R	1.80	1.90	2.00
θ	10° REF.		